A Collection of Technical Writing Sample Pages.

(Because of the Confidential and Proprietary nature of some the documents, these pages are randomly taken from various documents.)

Sample Pages from Micron Data Sheets

DDR2 SDRAM VLP SORDIMM

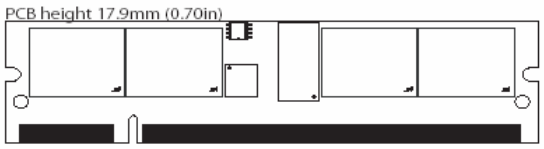
MT18HVS25672RH – 2GB

For component data sheets, refer to Micron's Web site: http://www.micron.com

Features

- 200-pin, very low profile small outline, registered, dual in-line memory module (VLP SORDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200 or PC2-5300
- 2GB (256 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- PLL to reduce system clock line loading
- Gold edge contacts
- Dual rank
- I^2C temperature sensor

Figure 1: 200-Pin VLP SORDIMM (MO-224)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 200-pin DIMM (Pb-free)	Y
• Frequency/CAS latency[2]	
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)[3]	-40E
• PCB height	
– 17.9mm (0.70in)	

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 5: Pin Descriptions

Symbol	Type	Description
ODT0	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
S0#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
A0–A13	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
DM0–DM8	Input (SSTL_18)	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
SCL	Input (SSTL_18)	**Serial clock:** SCL is used to synchronize the presence-detect and temperature sensor data transfer to and from the module.
SA0–SA1	Input (SSTL_18)	**Serial address inputs:** These pins are used to configure the presence-detect and temperature sensor devices.
RESET#	Input (LVCMOS)	Disables the output clocks on the PLL when LOW.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
CB0–CB7	I/O (SSTL_18)	Check bits.
DQS0–DQS8 (DQS0#–DQS8#)	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O (SSTL_18)	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect and temperature sensor devices.
EVENT#	Output (SSTL_18)	Temperature sensor alarm output.
V_{DD}	Supply	**Power supply:** +1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage.
V_{SS}	Supply	Ground.
V_{DDSPD}	Supply	**Serial EEPROM and temperature sensor positive power supply:** +3.0V to +3.6V.
NC	–	**No connect:** These pins should be left unconnected.

General Description

The MT18HVS25672RH(I) DDR2 SDRAM module is a high-speed, CMOS, dynamic random-access 2GB memory module organized in a x72 configuration. This DDR2 SDRAM module uses internally configured 8-bank (2Gb TwinDie™) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and re-drives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. The EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is tied to Vss on the module, permanently disabling hardware write protect.

1. INTRODUCTION to Electronic Compatibility

1.1 Scope

This document applies to the Commercial Avionics Systems (CAS) electromagnetic compatibility (EMC) or electromagnetic interference (EMI) design processes for the design of airplane electrical/electronic hardware. It provides guidelines of EMC/EMI techniques to be used by the designer on CAS designed equipment.

1.2 Purpose

The purpose of this document is to establish for the CAS hardware designer a uniform set of EMC/EMI design practices for the design of CM, PWB, PWA/SRU, and LRU hardware. Use of these design guidelines early in the design process will help to ensure the airplane EMC/EMI design requirements are met in a consistent manner at minimum cost.

1.3 EMC/EMI Design Process Overview

Figure 1.3-1 identifies the overall CAS H/W design process phases and the major EMC/EMI design tasks associated with each design phase.

During the Conceptual Design Phase the H/W and EMC/EMI designers develop the overall EMC/EMI design approach. Communications parameters are identified, such as, type of data, data buses, and the speed of signal. The interfaces to airplane functions are specified and operating modes are identified. The preliminary EMC/EMI requirements are analyzed and allocated to the functional elements of the conceptual design. These activities are accomplished in concert with System Engineering. EMC/EMI design approaches are defined for grounding/bonding, cable design, enclosure design, and circuit design.

During Preliminary Design, the H/W designer uses the conceptual design approach and requirements data to further define/allocate the EMC/EMI requirements for incorporation in the HWRD, and development of the preliminary design.

The Detail Design phase then takes the preliminary design data and develops detailed circuit schematics and hardware design data. The EMC/EMI design is reviewed for compliance with requirements and documented in the HWDD. This data is used to build initial hardware used in testing.

The Design Verification phase verifies design concepts by test, and ensures compatibility with the airplane and its electromagnetic environment.

The Red-Label phase further refines the previous design work to build hardware that will be used in full qualification testing. Once fully qualified, the Black Label (production) program proceeds.

1.0 Introduction the Sample System

1.1 Purpose

The purpose of this document is to provide the objectives of the project, the scope, and describe the current situation of the Sample System for historical purposes.

1.2 Information Asset Protection Policy

This document conforms to the Computerized Systems Validation Policy (CSVP) version 3.0 of the *Information Asset Protection Policies* (IAPP) manual, which states the following:

> A statement of the current situation will be written to provide a historical reference documenting the rationale for the project.
>
> The current situation may be documented as a part of a project justification (request for capital) or as a part of a requirements document. This is a historical product.

1.3 Objective

The objective of the Sample System is to continue to support the tracking of all events related to sample accountability for a sales representative in accordance with FDA and DEA legislation.

In addition, it is the objective of the Sample System team to complete the 1999 Sample Regulations Project. The purpose of this project is to implement changes to business and information systems that will the Company to be compliant with the new regulations published in December 1999. The changes include but are not limited to changes to:

> Business procedures
>
> Internal systems
>
> Field systems
>
> Interfaces
>
> Purchased data
>
> Packaging

The complete Purpose, Scope and Approach to the 1999 Sample Regulations Project are explained in detail in the *1999 Sample Regulation Charter*, which supports this *Statement of Current Situation*.

It is also the objective to update the Sample System's validation documentation, including some retrospective validation deliverables needed to become compliant with CSVP.

1.4 Scope

This *Statement of Current Situation* applies to the validation of the Sample System developed by the US Demand IT department, Technology Center, in association with the New Regulations Compliance Committee, Compliance, Manufacturing, QA, Legal, and Distribution.

1.5 Current Situation

The Sample System process has been developed to support the tracking of all events related to sample accountability for every sales representative at the Company in accordance with FDA and DEA legislation. These events include the shipment of sample product, the receipt of a shipment, the delivery of product samples, the return of product samples, the receipt of returned product samples, the theft and loss of product samples and the re-allocation of product samples from one representative to another representative. In addition, the system also supports the tracking of shipments directly to authorized physicians.

In December 1999 draft regulations were changed and finalized. All manufacturers must comply by December 2000. These regulations state that samples must be tracked down to the lot number. Currently lot numbers are printed on the packages and tracked to the sales representative. The lot numbers are not currently tracked manually or otherwise to the physician level. The new regulations also state that manufacturers must validate that a medical professional is eligible to receive samples per state law. Currently the Sample System team is obtaining these license numbers, improving the lot number tracking, and developing procedures for this validation process. The new FDA regulations describe what data must be gathered on requests and receipts. Most of this data is currently captured in our systems and/or documentation. We will be compliant with these new regulations before December 2000.

Testing is the process with the primary purpose of detecting errors and demonstrating that a system meets requirements and design specifications.

There are six processes of testing in the e-Data Management Program:

Development Testing	This is informal testing conducted during the development of a system or component, usually in the development environment by the developer.
Unit Testing	This is formal testing and debugging of the smallest functional part of a program. It focuses on the early examination of the functionality of units of code, ensures that functionality not visible at the system or acceptance level is examined by testing, and pinpoints discrepancies between what an application software component does and what it is expected to do. Paths, conditions, ranges, limits and algorithms as written in the source code are tested. A person other than the one who coded it must conduct this Unit testing.
Integration Testing	This is an orderly progression of testing in which software elements, hardware elements, or both, are combined and tested to evaluate their interactions until the entire system has been integrated. It ensures that relationships between units, and external interfaces, properly function and perform according to the design specifications.
System Testing	This is the process of testing an integrated hardware and software system to verify that the system meets its specified requirements, and demonstrates the application's ability to meet the business objectives and system requirements. This includes testing of security, ER/ES and performance requirements, and functional testing that challenges the intended use of the system. This is a CSV required testing level and must be conducted on a qualified platform that emulates the production environment.
Acceptance Testing	This is formal testing conducted by the system owner or designee to determine whether or not a system satisfies its original business objectives as described by the requirements documentation, and to enable the customer to determine whether or not to accept the system. It also must be conducted on a qualified platform that emulates the production environment.
Regression Testing	Regression testing usually is performed by rerunning test cases to detect errors because of changes or corrections made during software development and maintenance. This testing is conducted to ensure system change(s) implemented will not have adverse effects on other related parts of the system. Regression testing may also be performed by updating existing or creating new test cases.

3.2 Requirements Allocated to LRUs

EMC/EMI requirements are usually specified or allocated to CAS equipment at the LRU level. Requirements defining both EMC/EMI performance and hardware configuration are normally imposed.

3.2.1 EMC/EMI Performance Requirements

EMC/EMI performance requirements are specified by BCAG/FAA usually in terms of LRU limits for radiated and conducted susceptibility, and for radiated and conducted emissions.

a. Radiated susceptibility — these limits are based on the emission levels of all nearby radio and radar transmitters, including those installed on the airplane. They specify the component's required radiated susceptibility threshold level, below which it shall not be susceptible to radiated emissions.

b. Conducted susceptibility — these limits are based on the interference present on airplane power and signal systems and interference that can be coupled from nearby airplane cabling. They specify the component's required conducted susceptibility threshold level, below which it shall not be susceptible to conducted emissions. They are usually specified in voltage/current as a function frequency.

c. Radiated emissions — these limits are based on the threshold levels of intentional airplane receivers. They specify the component's required radiated emissions limit, above which radiated emissions shall not be allowed. They are usually specified in dBμV/M for narrowband, and dBμV/M/MHz for broadband emissions.

d. Conducted emissions — these limits are based on the threshold levels of equipment that can be coupled to through-interfacing cabling. They specify the component's required conducted emissions limit; above which conducted emissions shall not be allowed. They are usually specified in voltage peak-to-peak as a function of frequency.

If the requirements are correctly applied, and if the LRU complies with the limits, then the LRU should be compatible with the airplane operational interference environment.

System EMC/EMI requirements are specified in the documents listed in Section 2, Applicable Documents.

As an example, Table 3.2-1 lists the EMC/EMI requirements imposed on the 777 Cabin Management System (CMS) equipment. These requirements are typical of the requirements levied on electronic equipment on airplanes. The following code is used for the table:

1. INTRODUCTION to PWB/PWA Drawing Design Guide

1.1 Scope

The PWB/PWA Drawing Design Guide defines the standard process for creating new fabrication drawings. This process makes use of a series of pop-up menus and sub-menus developed to save time and ensure a higher quality product. It uses an Apollo/Mentor Board Station.

1.2 Purpose

The purpose of this document is to guide the designer through the steps and functions needed in setting up FABLINK, completing tasks before creating the fabrication drawings, and checking and releasing the new drawings.

This document also describes and illustrates the numerous menu options developed to simplify the process.

It is the responsibility of each designer or group involved in this process to follow these guidelines. This will ensure a complete and accurate board design in the shortest amount of time with the highest quality.

Appendix A FABLINK® PROCESS MENU DESCRIPTIONS

This section contains detailed descriptions of the menus used in the FABLINK drawing process. The shaded areas indicate the menu options selected for the step being described.

1.1 Reload Design Information

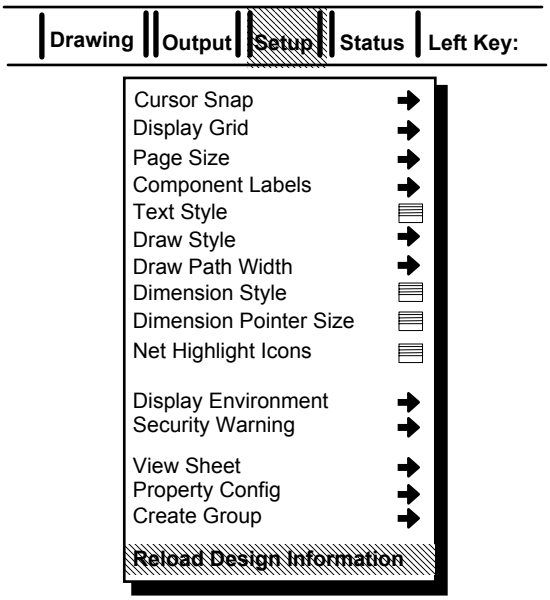


Figure A-1 Reload Design Information

Before FABLINK can create the manufacturing drawings, information specific to the design must be provided. This information includes: the number of layers; the existence of a paste mask; board, assembly and model numbers; etc. FABLINK receives this information from two files under the design directory:

a. **default_artwork_stackup**

b. **data_file**

FABLINK draws this design information from these two files at startup. If the information in either file is changed during a FABLINK session, the latest design specific information must be reloaded into FABLINK. The **Reload Design Information** menu option has been provided for this reason.

> NOTE: The **Reload Design Information** menu option is functional only if these two files exist in your system.

1.2 Create CAS Drawings

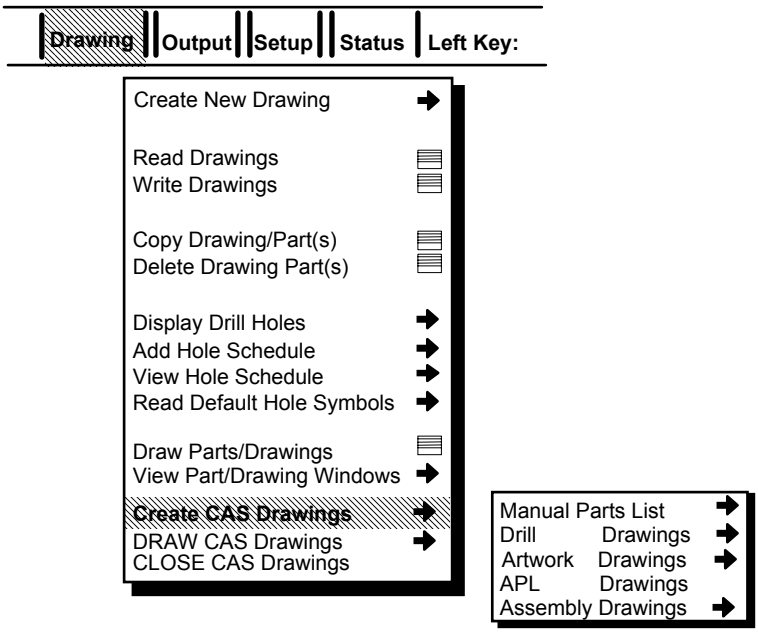


Figure A-2 Create CAS Drawings

The **Create CAS Drawings** menu option instructs FABLINK to create all drawing parts that begin with **dr_**. When the drawing contains artwork, the following three things are checked:

a. If the Gerber file does not exist, the appropriate graphics files are converted to Gerber format.

b. If the artwork does not exist, the Gerber file is viewed into FABLINK (for Signal Planes).

c. If the **artwork.true** part does not exist, the true artwork is created from the Gerber file (for Power Planes).

> NOTE: The **Create CAS Drawings** menu option and all sub-menu options, except **Create APL Drawings**, do not affect drawings already created.

1.2.1 Create Manual Parts List

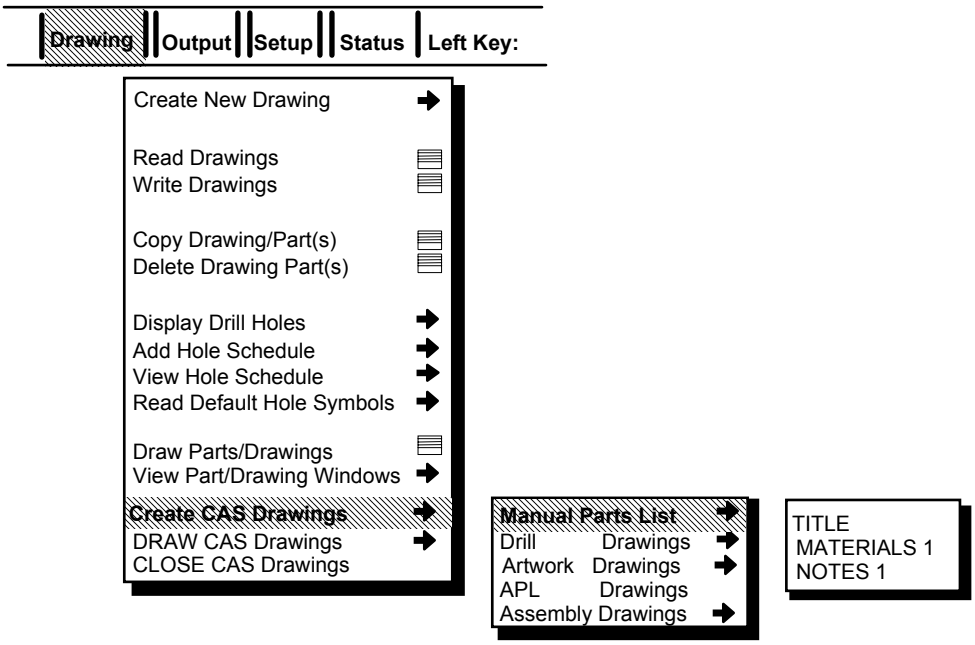


Figure A-3 Create Manual Parts List

The **Manual Parts List** sub-menu option instructs FABLINK to create all drawing parts that begin with **dr_pl_**. A second sub-menu allows the user the option to create one parts-list drawing part at a time.

2.0 Overall Test Plan

2.1 Test Processes

The Test Process begins with planning once the business requirements have been defined, approved and committed to by the client and ends when the system is accepted by the client after acceptance test, and reoccurs as changes are made during maintenance or enhancements. The Test Process interfaces extensively with the:

Clients who are involved in planning and conducting acceptance tests and possibly other levels of test; **Analysts** who are the users of the process; **Management** who receives information on the quality of the products under test;

Requirements Process defines the business and system requirements that are verified by the test process;

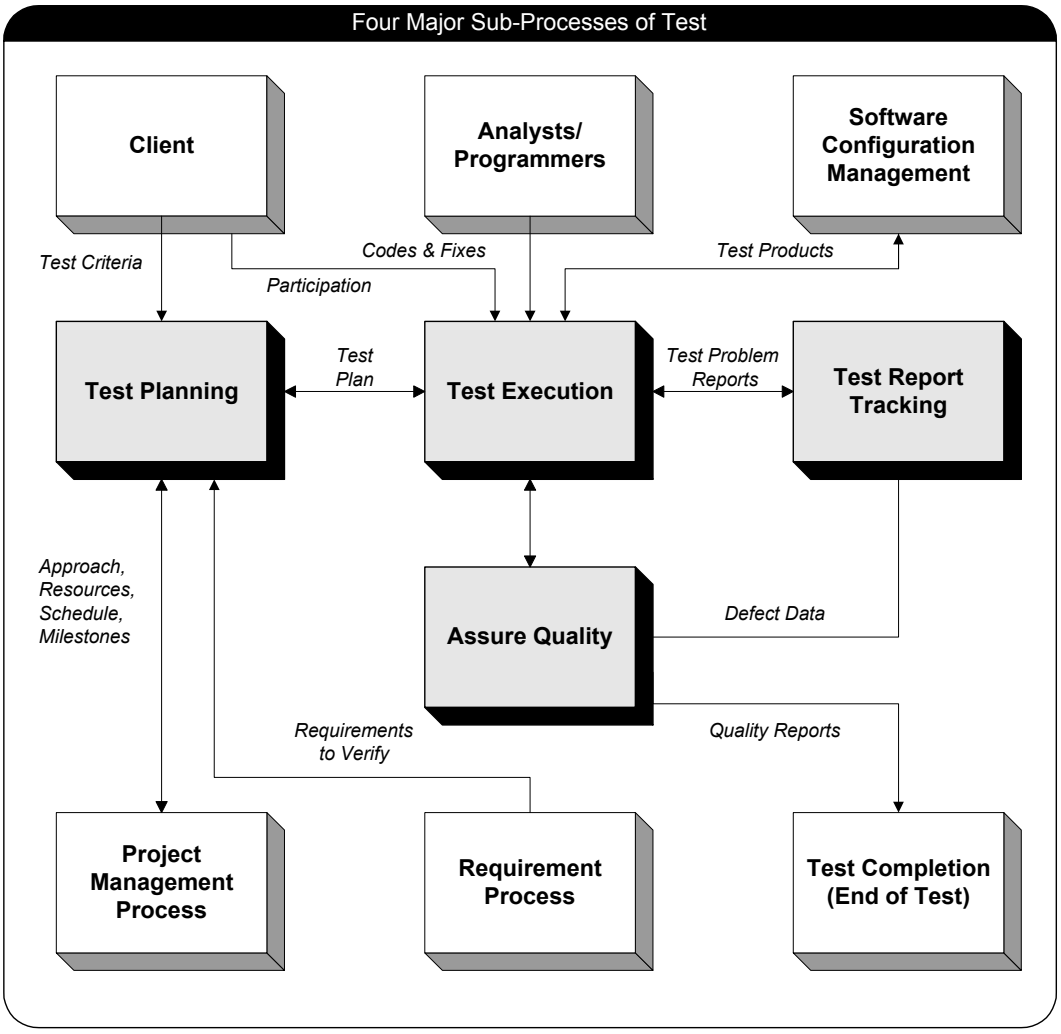
Project Management Process that integrates the project specific Test activities, methods, and status with other project aspects, forming an overall Project Plan and project status; and

Software Configuration Management Process that controls different versions undergoing test, associated test products and tools

This section defines the Test Process by defining four major sub-processes.

Test Planning
Test Execution
Problem Report Tracking
Assure Quality

The Figure below illustrates the relationship among the four major sub-processes.



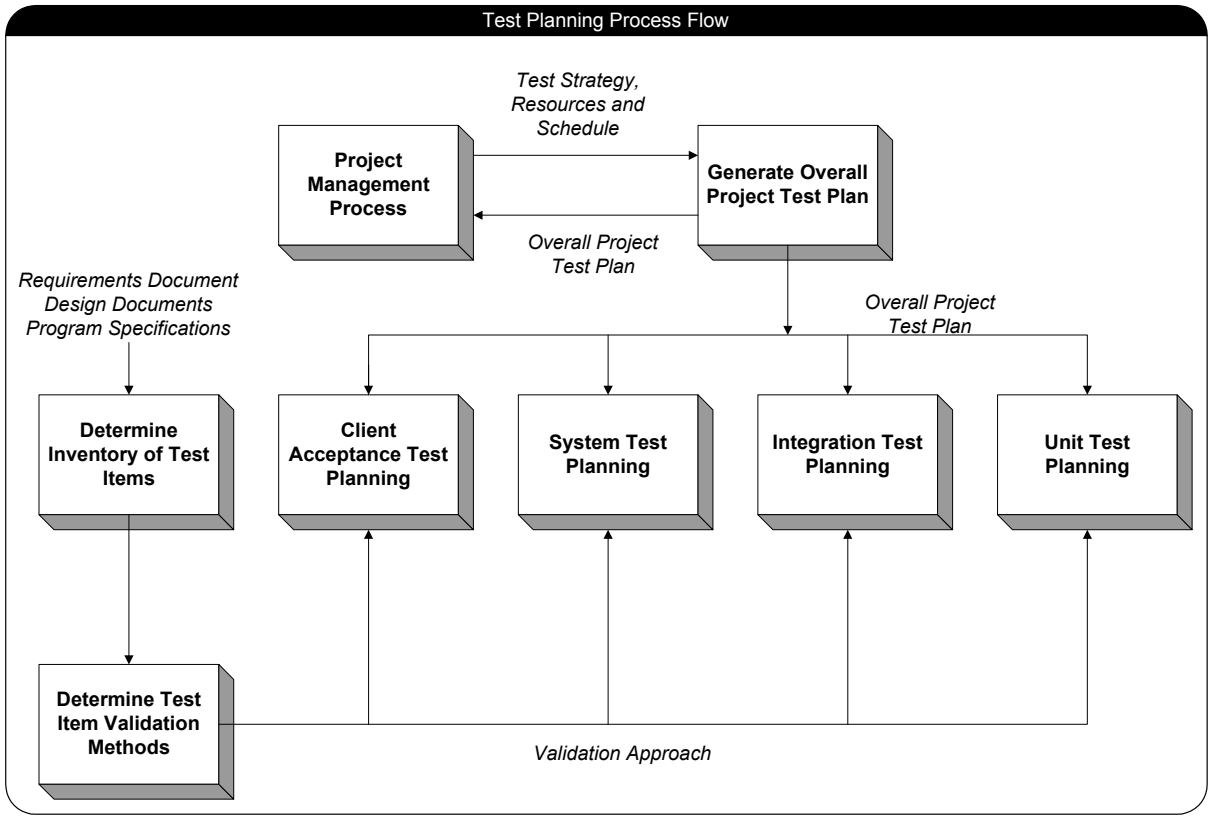
2.1.1 Test Planning

Test Planning defines all the activities for planning a project's test strategy and approach, and planning those tests that will verify the system. Test Planning results in the project specific application of the Test Process, including the:

project's test approach, activities, summary schedule, and organizational and management aspects, identified in the Project Plan;
preparation of a test environment including necessary hardware, test tools and test data,
verification method for each business, system and software requirement, and the test levels in which it will occur; and

development of test plans for each Test , including the identification of *Test Items*, *Test Categories* and the identification of *Test Cases* that will specify what types of tests will be conducted.

Test Planning is an activity that is a necessary preparation for the actual testing of the system or process. In general, testing is planned in a "top down" fashion starting with an overall plan. Planning next occurs for the entire system through the lower levels of integrated units to the individual software units themselves.



2.1.2 Test Execution

Test Execution defines all the activities for conducting and reporting test results for each test level (unit, integration, system, client acceptance). Test Execution includes:

preparing *Test Scripts* that identify the steps and expected results of each Test Case;

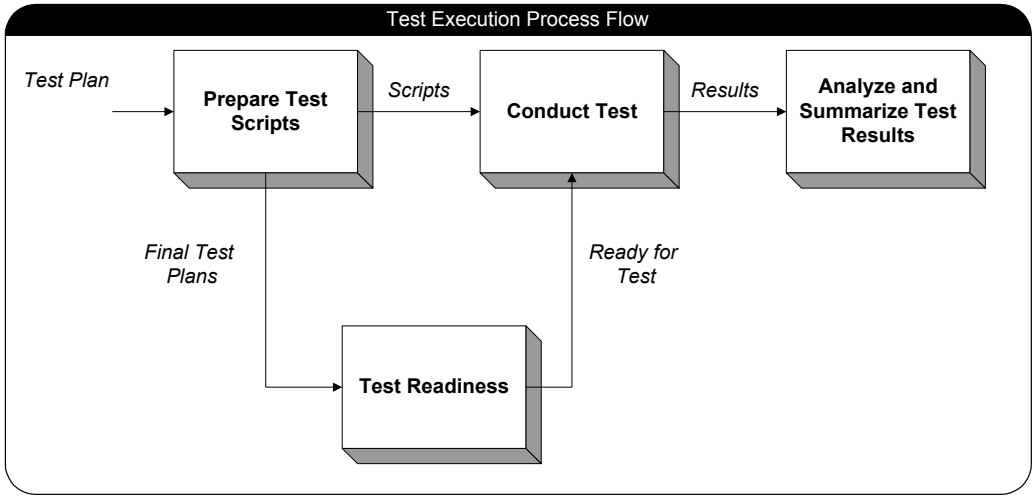
conducting a *Test Readiness Review* prior to System and Client Acceptance Test to ensure all preparations has been accomplished;

executing the specific tests in accordance with the Test Plan and Scripts; and

documenting the status of the *Test Effort*.

Test Execution is the activity which conducts, analyzes and summarizes the results of software testing to verify that the system's internal logic and

design satisfies the system requirements. Its purpose is to identify and fix defects during development BEFORE the system is delivered to the customer.



2.1.3 Problem Report Tracking

Problem Report Tracking defines the activities for reporting, assigning and closing problems that occur during System and Acceptance Test. This includes: establishing a Problem Reporting System to collect and track Problem Reports; initiating Problem Report when problems are identified during test; correcting the problem and closing the Problem Report; and problem root cause analysis to improve both the test and development processes.

Test Problem Report Tracking is the activity for reporting, assigning, fixing and closing software problems that occur during the *Formal Testing* levels (System and Client Acceptance). Although not required, this procedure could be used to log test problems during the *Technical Testing* levels (Unit and Integration).

1. INTRODUCTION to Creating & Releasing Documentation

1.1 Scope

This document establishes the CAS process for creating and releasing engineering documentation, which is in the form of either a document (e.g., HWRDs, HWDDs or design guidelines) or a book-form drawing, for hardware designs and design processes. It is based on existing procedures and provides the functions to be followed and completed to ensure a document or book-form drawing has met all the procedural and technical requirements. It defines the steps for creating the document or book-form drawing from its initial identification and definition, through its final release and storage.

This document will be concerned with two areas of documentation; documents, and book-form drawings. In most cases the procedure is the same for both and in this document they will be addressed together as documentation. Where the procedures for documents and book-form drawings differ they will be addressed separately.

1.2 Purpose

The purpose of this document is to standardize the procedure and format for creating documentation needed in the CAS engineering design process, and not the content of documentation, which is defined in other documents. When a new or revised document or book-form drawing is released, it is essential that it be complete, accurate and controlled. In this document, when the text refers to a drawing, it means a book-form drawing. This document does not replace the already existing documents that define standards, but supplies an outline to assist the originator of documentation. It helps to ensure that all procedures and standards are complied with while developing H/W design-process documentation.

1.3 Overview of the Process Flow

Figure 1.3-1, H/W Design Documentation and Release Process, illustrates the overview of the process. This includes:

a. Determining the need of documentation, document or drawing

b. Identification of the documentation

c. Creation of the documentation on the selected platform

d. Review and approval

e. Release and storage

3.1.4.4 Notes Concerning Document Creations

The following are notes and hints of which the user should be aware when creating a document in Mentor.Doc and using the BDS-2065 standards template.

a. Do not substitute spaces for tabs. Spaces are text dependent and they will not be constant from paginate to paginate.

b. If the line spacing is inconsistent from line to line with stretched format codes, verify the nominal font size and execute the associated menu, **layout > set nominal font**

c. Verify the path is correct when updating tables or figures. If the path is incorrect, the table or figure will disappear from your file.

d. Creation of Appendices

(1) style sheet **num_section_style_s**

(2) Menu **create > section > show as Appendix,** at the point in the document the appendix will be inserted.

- Hide section and title — Select (**yes**).
- Include in table of contents — Select (**yes**).
- Execute the menu.
- Type APPENDIX **number** within the Appendix format codes. Insert a **center** format code.
- Triple space below APPENDIX **number** and type the appendix title (see BDS-2065 for formatting the Appendix title).

(3) Page numbering by section **template > page > page numbering > by section.**

(4) Table and Figures are numbered by section number **template > tables > by section** or **template > pictures > by section**

3.1.4.5 Determine Mentor File Name and Path

The CAS directory structure for the given design determines the Mentor file name and path. All project support documents will be developed in the appropriate place in the Mentor directory under the appropriate LRU, SRU, or CM.

3.1.4.6 Changing and Updating Existing Mentor Documents

The following steps define the process for updating existing online Mentor.Doc documents to ensure they meet the BDS-2065 standards:

a. Delete from the existing template the section, list, page, and other generic format codes.

b. Run the **update_pages** macro within your "DOC" session. This will reset the page layout and invoke the /user/proj/doc/bds_templates/def_style_s style sheet. Verify the

style sheet using **template - style - other - style sheet name "menu"**

The style sheet can be changed depending on the number of indenture levels required, or if the document requires more than one volume. See Section 3.1.4.3, which describes dividing a document into more than one volume. The following shows changes that can be made to the indenture levels:

(1) For five levels of subsection of indenture, use
/user/proj/doc/bds_templates/def_style_s

(2) For three levels of subsection of indenture use
/user/proj/bds_templates/bds_style_l4_s

(3) For documents with volumes
/user/proj/doc/bds_templates/volume_style_s

c. Change listing bullets into alphanumeric lower case per BDS-2065 standards.

d. Comply with the deviation written to allow the subsequent text of lists and items to line up under the first line of the text, rather than under the lower-case letters or numbers that identify the sections.

e. Add the appropriate Generic Title page, Active pages, Revision page, Footers, and Headers using the command **Add_bds_pages** in the command window within a "DOC session". Highlight the command and press the **shell/cmd** key, select the appropriate item.

3.1.5 Distribution of a First Draft for Review

The originator is responsible for developing a first draft copy of the document. After the data has been input, and the graphics completed and inserted, the originator develops a first-draft copy of the document. The first draft should follow the original outline as close as possible.

The first-draft copy of the document is distributed by the originator to the key personnel and to the SMEs for review. They are responsible to ensure the accuracy of the content and furnish the originator with concise notes, critique, added information, or corrections. Following are several optional methods for distribution and response of the document to the key personnel.

1.0 Introduction ARIIS User's Manual

1.1 Purpose

The purpose of this User's Manual is to provide basic operation guidelines that focus on the Automated Rivet Interference Inspection System (ARIIS) processes that affect rivet inspection.

1.2 Scope

The ARIIS was developed to replace the time-consuming, inaccurate methods of measuring rivet interference for machine-installed fluid-tight applications. ARIIS uses four main components that work collectively as an automated measurement system. The four components are: a single-axis stepper motor, a bench center, a laser micrometer, and a PC computer.

The ARIIS system runs on built software built and, written in "C" programming language, which instructs the stepper motor to move the rivet to precise locations and take laser measurements at those locations.

The ARIIS rivet inspection is currently being used in Everett, as well as the East and West Factories in Renton, in production for 737, 747, 757, 767, and 777 wing riveting operations. Spin-off applications are forming with the inspection of cold work mandrels for wear, receiving and inspection of new mandrels, generic inspection of multiple fastener types, inspection of fluid-tight Low-Voltage Electromagnetic Riveting (LVEMR) install rivets, and as a tool to be used in conjunction with laboratory research.

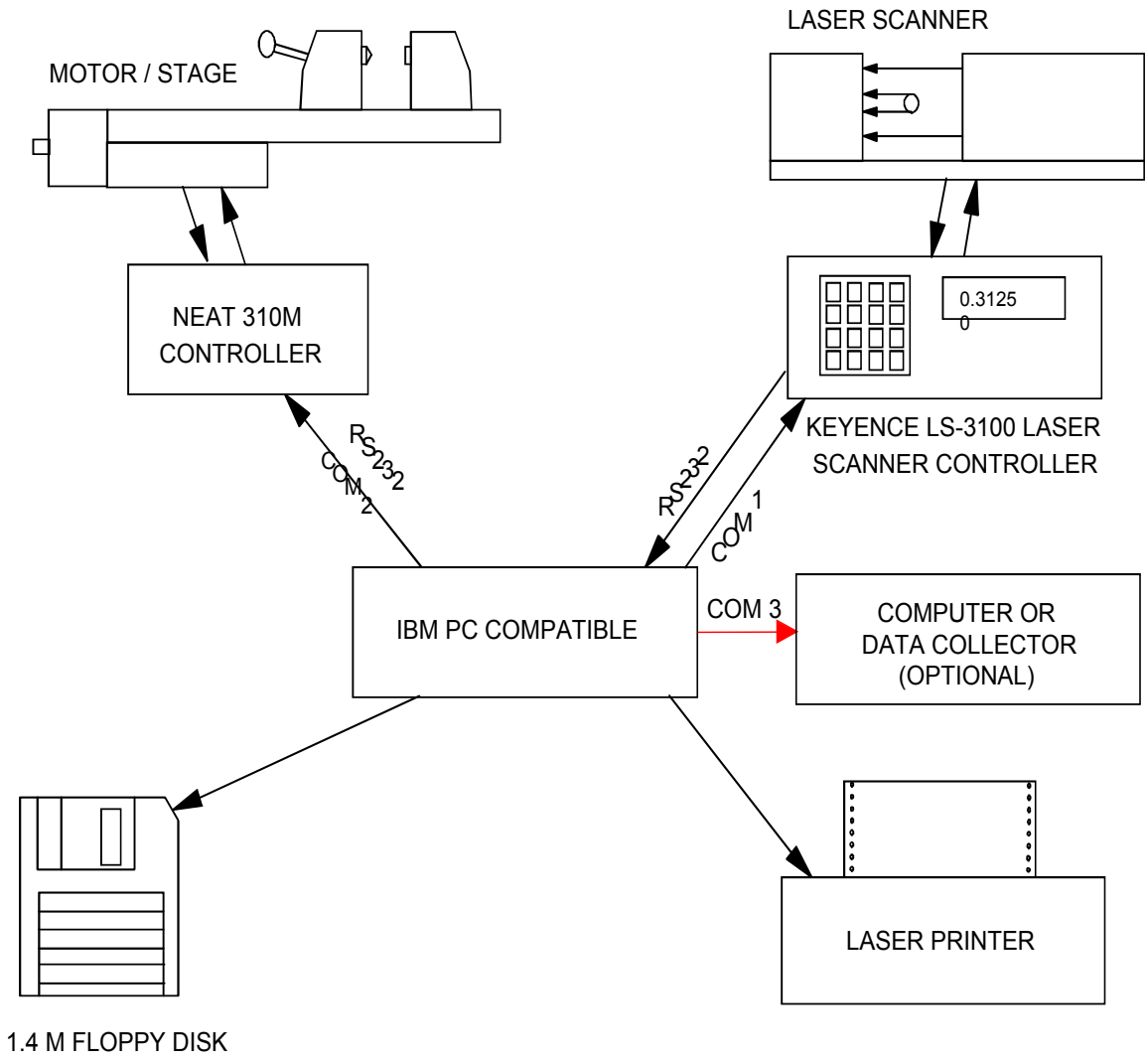


Figure 2.1 Hardware Configuration

2.1.1 Keyence Laser Scanner

The Keyence laser scanner is a commercially available product that is capable of very precise diameter measurements. It consists of a laser source that scans to produce a collimated "plane" of laser light that is roughly 2.5 in wide. A receiver collects this laser light and detects breaks in the beam. There are four modes of measurement provided. Refer to figure 2.2. The ARIIS software uses all four modes. Direct diameter measurements are made using mode one for measurement of D1-D4 and button diameter. Indirect diameter measurement is used for countersink diameter measurement and is made by subtracting measurements in modes three and four from the measurement in mode two. The ARIIS software automatically configures the laser scanner to average 32 scans for each measurement. This is a speed/accuracy trade off. The MANUAL.EXE program uses the maximum 1024 scan averaging.

MAIN MENU item “4> Profile Plots” allows the user to recall the latest profile plot for any coupon. This profile can be sent to the printer or saved to a floppy disk (if the ASK TO SAVE. option is set).

The INTERFERENCE PLOTS utility allows the user to display up to five interference plots simultaneously. This is useful for comparison purposes. When this is selected from the HOST MENU, the user is asked for the number of profiles to plot. The next query is for a plot title. The program will then request whether the profiles are in disk drive **A:** or **B:**. When this is complete, the filenames for the profiles will be requested one at a time. The profiles will then be plotted with the title at the top and a legend on the right identifying the profiles by file name. The plot can be sent to the printer with the <Print Screen> key.

2.7 Accessing SQC data (Control Charts and Histograms)

MAIN MENU items “5> Production SQC files”, and “6> Qualification SQC files”, allow the user to access data from the 50 most recent runs of any production or qualification coupon respectively. When these are executed, the user must select a coupon from the menus in the same manner as when inspecting a coupon. The data file for the selected coupon is opened and nine SQC files are generated automatically. The SQC program is then automatically loaded. By selecting **File** and then **Open** from the SQC menu, the following files will be available: BTHEIGHT, BTNDIA, CSK, CSKDIA, D1, D2, D3, D4, and HOLEDIA. When one of these files is selected, the data can be viewed directly by selecting **Edit** from the SQC menu. To enter or edit specification limits or title information, select **Options** then **Data File** from the SQC menu. By choosing **Chart**, a menu of available plots is listed. When a plot is selected and displayed, several display options are available by typing the letter “**o**” while the plot is displayed. To print a plot, press <**Alt P**> while the plot is displayed. Before printing a plot, ensure the printer selection is correct and that “fast print” is turned off. To do this, select **Options** then **Printer** from the SQC MENU and verify the printer is 'HP Laser Jet' and that 'Fast Print?' says 'NO'. To make changes of these entries, press the **Down Arrow** to the one to change, then press the **Right Arrow** key to change the selection until it is correct. Press <**Esc**> to exit SQC MENU.

2.8 Calibration/Certification

This section describes the actions required to calibrate and certify both the Keyence laser scanner and the NEAT 310M motor controller. This is essentially a duplication of the on-line procedure that is available from the CAL/CERT MENU in the ARIIS software.

Procedure:

1. Exit the ARIIS program to DOS (The Cal/Cert password will work. Initially, it is “cc”). Ensure the prompt is **C:\ARIIS>**.

2. Execute **"attrib -h -r cal_fact.dat"** to unprotect the calibration file for updating. If cal_fact.dat does not exist (startup), proceed to step 4.

3. Verify the contents of the CAL_FACT.DAT, and the RI.EXE or EV.EXE files. Insert the cal/cert diskette that contains controlled copies of these files and execute **comp a:cal_fact.dat cal_fact.dat** and **comp a:ri.exe ri.exe** (Renton) or "**comp a:ev.exe ev.exe** (Everett). File comparisons should check out OK. If not, contact the responsible Facilities personnel.

4. Type **menu** to enter the ARIIS HOST MENU, select "ARIIS" and type the Cal/Cert password to enter the ARIIS MAIN MENU. Select **Calibration/Certification**

and enter the cal/cert password to reach the CERTIFICATION MENU. Execute Keyence scanner calibration and motor/stage certification as described in the details below.

5. Return to DOS, insert diskette, type **copy cal_fact.dat a:**. Remove and retain the diskette when complete.

6. Type **attrib +h +r cal_fact.dat** to protect it. Type **menu** to return to MAIN MENU. Calibration is complete.

2.8.1 Calibration and Certification of the Keyence LS-3100 Laser Scanner

Four diameter standards of at least ±0.000025 in quality (cyclindricity) are required. Nominal diameter standards required are 0.1875, 0.2500, 0.3125 and 0.3750 in. When **1> Calibrate Keyence Laser Scanner** is selected from the CAL/CERT MENU, the computer will ask for the actual diameter of the first standard. When this value is entered, it will prompt for the clean standard to be placed in the chuck. When this is done, press <**Enter**> and the ARIIS will make 50 direct and indirect measurements of the standard. The program will then execute a "**t**" statistic test. If it finds a significant difference (95% confidence) between the mean of the direct or indirect measurements and the actual for the standard, a calibration factor(s) will be stored for that nominal diameter. The program will then make another 50 measurements of the standard using the calibration factors and report the minimum and maximum values. If any of the measurements exceed the nominal plus or minus 0.0001 in, clean the standard and start over. This procedure will be repeated until all four standards have been calibrated and 50 calibrated measurements (direct and indirect) are within acceptable range.

2.8.2 Certification of NEAT 310M Motor/Stage

Stage displacement must be measurable within 0.0005 in. Select **2> Motor/Stage Certification** from the CAL/CERT MENU. The system will enter the certification utility mode. Follow the instructions to adjust the jog increment and move the stage left and right. Position the motor/stage so the laser roughly intersects the rightmost portion of the measuring envelope. (This is where the rivet contacts the right (or fixed) chuck member.) Starting with the 0.1000 in increment, zero the accumulator <**F10**> then step ten steps to the left and ten steps to the right. Verify the accuracy of each motion. Repeat this procedure for jog increments of 0.0100, 0.0010 and 0.0005 in. All movements must be within 0.001 in of predicted.

Note: The motor certification utility is useful for spot checks on laser scanner accuracy. Press <**Enter**> and direct and indirect measurements are made that use the appropriate calibration factors. All measurements taken with this utility should comply to within .0001 in of actual.